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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/083,261	02/25/2002	Joon-Hoo Choi	8071-12 (OPP 011059US)	7814

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EXAMINER	
WANG, GEORGE Y	
ART UNIT	**PAPER NUMBER**
2871	

DATE MAILED: 08/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/083,261	CHOI ET AL.	
	Examiner	Art Unit	
	George Y. Wang	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,7-12 and 33-56* is/are pending in the application.

4a) Of the above claim(s) *41-56* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,7-12 and 33-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
> This application currently names joint inventors.

In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

2. Claims 1, 7-9, and 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gu et al. (U.S. Patent No. 5,920,084, hereinafter "Gu") in view of Murakami et al. (U.S. Patent No. 5,053,844, hereinafter "Murakami").

3. As to claim 1, Gu discloses a thin film transistor array substrate comprising an insulating substrate (fig. 6, ref. 9), a first signal line (fig. 6, ref. 17) formed on the

insulating substrate, a first insulating layer formed on the first signal line (fig. 6, ref. 21), a second signal line formed on the first insulating layer while crossing over the first signal line (fig. 6, ref. 13, 15), a thin film transistor (TFT) connected to the first and second signal lines (fig. 6, ref. 23), a second insulating layer formed on the TFT with a first contact hole (fig. 27) exposing predetermined electrode of the TFT and having a dielectric constant about 4.0 or less (abstract; col. 7, line 65 – col. 8, line 18), and a first pixel electrode (fig. 6, ref. 3) formed on the second insulating layer while being connected to the predetermined electrode of the TFT through the first contact hole (fig. 6, ref. 35; col. 10, line 66 – col. 11, line 5). Gu further discloses a TFT array substrate (abstract) as recited above with a second insulating layer formed with an a-Si layer.

However, the reference fails to specifically disclose a second insulating layer formed with an a-Si:C:O or a-Si:O:F layer.

Murakami discloses an insulating a-Si layer formed with an a-Si:O:F layer (fig. 8, ref. 403).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have formed a second insulating layer formed with an a-Si:C:O or a-Si:O:F layer since one would be motivated to use these well known amorphous silicon materials to reduce the band gap thickness, which ultimately increases the intensity ratio, improves uniformity in structure, and maximizes color-sensing application (col. 2, lines 43-48).

4. As to claims 7-8, Gu discloses an a-Si TFT array substrate as recited above (abstract), however, the reference fails to specifically the a-Si layer being formed by a PECVD method.

Murakami discloses an a-Si TFT array substrate formed by a PECVD method using an oxide agent (col. 5, lines 6-11).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have an a-Si TFT array substrate formed by a PECVD method using an oxide agent since one would be motivated to reduce the band gap range to a level that optimizes sensitivity to light having short wavelengths (col. 6, lines 9-22). This is creates a more preferable range that ultimately increases the intensity ratio, improves uniformity in structure, and maximizes color-sensing application (col. 2, lines 43-48).

In addition, even though the product-by-process limitation "is formed through plasma enhanced chemical vapor deposition (PECVD)..." is recognized as limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior art product was made by a different process. *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985). See also MPEP 2113.

5. As per claim 9, Gu discloses a TFT array substrate as recited above where the second insulating layer has a dielectric constant of about 2 to about 4 (abstract; col. 7, line 65 – col. 8, line 18).

6. Regarding claims 11-12, Gu discloses a TFT array substrate as recited above where the pixel electrode is made of an optically transparent and electrically conductive material such as ITO (col. 8, lines 21-22).

7. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gu and Murakami in view of Dohjo et al. (U.S. Patent No. 5,646,756, hereinafter "Dohjo") and Ono et al. (U.S. Patent No. 5,668,379, hereinafter "Ono").

Gu discloses a TFT array substrate with a first insulating layer made of silicon nitride (col. 9, lines 58-64) and other materials with dielectric of 4 or less (col. 7, line 65 – col. 8, line 18) as recited above, however, the reference fails to specifically disclose a second bottom dielectric layer having a dielectric constant about 4 or less.

Dohjo discloses a TFT substrate having a first insulating layer with a top layer (fig. 1, ref. 20) made of silicon nitride and a bottom layer (fig. 1, ref. 16) made of a low dielectric material, such as SiOx.

Ono discloses a TFT substrate where SiOx has a dielectric constant about 4 or less (col. 19, lines 54-67).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have a first insulating layer with a top layer formed of silicon

nitride and a second bottom layer formed of a low dielectric material, such as SiOx, having a dielectric constant about 4 or less by optimizing film thickness (Ono, col. 19, lines 61-64) since one would be motivated to reduce vulnerability to the penetration of impurity ions into the transistor, which ultimately provides greater insulation for preventing deteriorated image quality (Dohjo, col. 3, lines 6-9; col. 2, lines 39-55).

8. Claims 33, 37, 39-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gu in view of Dohjo and Ono.

9. As to claim 33, Gu discloses a thin film transistor array substrate comprising an insulating substrate (fig. 6, ref. 9), a first signal line (fig. 6, ref. 17) formed on the insulating substrate, a first insulating layer formed on the first signal line (fig. 6, ref. 21), a second signal line formed on the first insulating layer while crossing over the first signal line (fig. 6, ref. 13, 15), a thin film transistor (TFT) connected to the first and second signal lines (fig. 6, ref. 23), a second insulating layer formed on the TFT with a first contact hole (fig. 27) exposing predetermined electrode of the TFT and having a dielectric constant about 4.0 or less (abstract; col. 7, line 65 – col. 8, line 18), and a first pixel electrode (fig. 6, ref. 3) formed on the second insulating layer while being connected to the predetermined electrode of the TFT through the first contact hole (fig. 6, ref. 35; col. 10, line 66 – col. 11, line 5). Gu further discloses a TFT array substrate (abstract) as recited above with a second insulating layer formed with an a-Si layer and

a TFT array substrate with a first insulating layer made of silicon nitride (col. 9, lines 58-64) and other materials with dielectric of 4 or less (col. 7, line 65 – col. 8, line 18).

However, the reference fails to specifically disclose a second bottom dielectric layer having a dielectric constant about 4 or less.

Dohjo discloses a TFT substrate having a first insulating layer with a top layer (fig. 1, ref. 20) made of silicon nitride and a bottom layer (fig. 1, ref. 16) made of a low dielectric material, such as SiOx.

Ono discloses a TFT substrate where SiOx has a dielectric constant about 4 or less (col. 19, lines 54-67).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have a first insulating layer with a top layer formed of silicon nitride and a second bottom layer formed of a low dielectric material, such as SiOx, having a dielectric constant about 4 or less by optimizing film thickness (Ono, col. 19, lines 61-64) since one would be motivated to reduce vulnerability to the penetration of impurity ions into the transistor, which ultimately provides greater insulation for preventing deteriorated image quality (Dohjo, col. 3, lines 6-9; col. 2, lines 39-55).

10. As per claim 37, Gu discloses a TFT array substrate as recited above where the second insulating layer has a dielectric constant of about 2 to about 4 (abstract; col. 7, line 65 – col. 8, line 18).

11. Regarding claims 39-40, Gu discloses a TFT array substrate as recited above where the pixel electrode is made of an optically transparent and electrically conductive material such as ITO (col. 8, lines 21-22).

12. Claims 34-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gu, Dohjo, and Ono, in further view of Murakami.

Gu, when modified by Dohjo and Ono, discloses an a-Si TFT array substrate as recited above (abstract), however, the reference fails to specifically the a-Si layer being formed by a PECVD method.

Murakami discloses an a-Si TFT array substrate formed by a PECVD method using an oxide agent (col. 5, lines 6-11).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have an a-Si TFT array substrate formed by a PECVD method using an oxide agent since one would be motivated to reduce the band gap range to a level that optimizes sensitivity to light having short wavelengths (col. 6, lines 9-22). This is creates a more preferable range that ultimately increases the intensity ratio, improves uniformity in structure, and maximizes color-sensing application (col. 2, lines 43-48).

In addition, even though the product-by-process limitation "is formed through plasma enhanced chemical vapor deposition (PECVD)..." is recognized as limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the

prior art, the claim is unpatentable even though the prior art product was made by a different process. *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985). See also MPEP 2113.

13. Claims 10 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gu, Murakami, Dohjo, and Ono, in further view of Sasano et al. (U.S. Patent No. 5,671,027, hereinafter "Sasano").

Gu, when modified by Murakami, Dohjo, and Ono, disclose a TFT array substrate as recited above where the first signal line is formed of alloys of Cr or Al (col. 10, lines 5-8).

However, the reference fails to specifically disclose that the first signal line includes a first and a second layer.

Sasano discloses a TFT substrate with a first signal line having a first layer (fig. 2a, ref. g1) made of Cr alloy (col. 13, lines 5-6) and a second layer (fig. 2a, ref. g2) made of Al alloy (col. 13, lines 18-19).

It would have been obvious to one of ordinary skill at the time the invention was made to have a first signal line having a first layer made of Cr alloy and a second layer made of Al alloy since one would be motivated to reduce short circuiting that leads to defects and deterioration (col. 1, lines 65-68) and to increase excellent display performance (col. 2, lines 16-18).

Response to Arguments

14. Applicant's arguments filed June 8, 2005 have been fully considered but they are not persuasive.

Applicant's main argument is that the combination of Murakami and Gu lacks motivation to combine. Applicant supports this contention by asserting that the advantages of Murakami to "reduce the band gap thickness, which ultimately increases the intensity ratio, improves uniformity in structure, and maximizes color-sensing application" are "not relevant" because the "purpose of the a-Si:O:F insulating layer is to reduce or minimize parasitic capacitance." However, in response to applicant's argument that the advantages taught by Murakami are "not relevant," the fact that applicant has recognized another advantage which would flow naturally from following the suggestion of the prior art cannot be the basis for patentability when the differences would otherwise be obvious. See *Ex parte Obiaya*, 227 USPQ 58, 60 (Bd. Pat. App. & Inter. 1985). Simply because Applicant has recognized that one purpose of the a-Si:O:F insulating layer is to reduce or minimize parasitic capacitance does not preclude such use of the insulating layer from advantages associated with reducing the band gap thickness, which ultimately increases the intensity ratio, improves uniformity in structure, and maximizes color-sensing application.

Applicant also argues that the combination of Gu, Dohjo, and Ono does not disclose a TFT array having "a first insulating layer includes a top layer and a bottom layer, the bottom layer having a dielectric constant about 4 or less, and the top layer beuin a silicon nitride layer," as essentially recited in claim 33. Applicant argues that the Dohjo reference does not teach a bottom insulating layer and asserts that layer 16 is

a semiconductor layer, which is different from an insulating layer. However, nowhere in the claim does it specify that the bottom layer must be an insulating layer. The claim merely recites that a first insulating layer includes a top layer and a bottom layer. Furthermore, when broadly interpreted, any layer, even a semiconductor layer can function to "insulate" one portion of the array with another. Even assuming that Applicant is correct, and that the Dohjo reference does not, in fact, teach or suggest a bottom insulating layer, the Ono reference clearly remedies the deficiency of Gu by disclosing a two-layer insulting structure, where the top layer is a silicon nitride and the bottom layer is formed of a low dielectric material, such as SiOx, having a dielectric constant about 4 or less (col. 19, lines 54-67).

As a result, Examiner holds to the validity of the references used and maintains rejection.

Conclusion

15. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to George Y. Wang whose telephone number is 571-272-2304. The examiner can normally be reached on M-F, 8 am - 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert H. Kim can be reached on 571-272-2293. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

gw
August 19, 2005

ROBERT KIM
SUPERVISORY PATENT EXAMINER